AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1-15 (Canceled).

16. (Currently Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in said integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one pre-designed circuit block ~~self-contained layout section~~ comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said pre-designed circuit block ~~self-contained layout section~~ comprising a routing of conductors developed independent from routing of conductors for circuits outside said pre-designed circuit block ~~self-contained layout section~~ in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of said metal layer in said second metal layer group directly adjacent to said pre-designed circuit block, wherein at least one conductor along said preferred diagonal direction on the metal layer directly above said pre-designed circuit block traverses across the boundaries of said pre-designed circuit block ~~self-contained layout section~~, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said pre-designed circuit block ~~self-contained layout section~~,

wherein said preferred Manhattan direction conductors of said pre-designed circuit block ~~self-contained layout section~~ within said first metal layer group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said pre-designed circuit block ~~self-contained layout section~~ conductors are deposed in either a horizontal or vertical direction; and

wherein said pre-designed circuit block ~~self-contained layout section~~ is ~~a section~~ less than the entire area of said metal layer in said first metal layer group.

17. (Currently Amended) The integrated circuit as set forth in claim 16, wherein said pre-designed circuit block ~~self-contained layout section~~ is independent of a layout for said second metal layer group.

18. (Currently Amended) The integrated circuit as set forth in claim 16, further comprising a plurality of pre-designed circuit blocks ~~self-contained layout sections~~ in said first metal layer group.

19. (Currently Amended) The integrated circuit as set forth in claim 18, wherein at least one of said pre-designed circuit blocks ~~self-contained layout sections~~ comprise a wiring direction perpendicular to a wiring direction of a second one of said pre-designed circuit blocks ~~self-contained layout sections~~.

20. (Canceled).

21. (Original) The integrated circuit as set forth in claim 16, wherein said first metal layer group comprises three metal layers.

22. (Previously Presented) The integrated circuit as set forth in claim 21, wherein said three metal layers comprise first, second, and third metal layers, each of said three metal layers comprising conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

23. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

24. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

25. (Currently Amended) The integrated circuit as set forth in claim 16, wherein said pre-designed circuit block ~~self-contained layout section~~ comprises a layout for a memory block.

26. (Canceled).

27. (Currently Amended) The integrated circuit as set forth in claim 16, wherein said pre-designed circuit block ~~self-contained layout section~~ comprises a section less than 10 percent of the entire area of said metal layer in said first metal layer group.

28. (Currently Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one pre-designed circuit block ~~self-contained layout section~~ comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said pre-designed circuit block ~~self-contained layout section~~

comprising a routing of conductors developed independent from routing of conductors for circuits outside said pre-designed circuit block ~~self contained layout section~~ in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of said metal layer in said second metal layer group directly adjacent to said pre-designed circuit block, wherein at least one conductor along said preferred diagonal direction on the metal layer directly above said pre-designed circuit block traverses across the boundaries of said pre-designed circuit block ~~self-contained layout section~~, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said pre-designed circuit block ~~self contained layout section~~,

wherein said preferred Manhattan direction conductors of said pre-designed circuit block ~~self-contained layout section~~ within said first metal layer group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said pre-designed circuit block ~~self-contained layout section~~ conductors are deposed in either a horizontal or vertical direction; and

wherein said pre-designed circuit block ~~self contained layout section~~ is a section less than the entire area of said metal layer in said first metal layer group.

29. (Currently Amended) The method as set forth in claim 28, wherein said pre-designed circuit block ~~self contained layout section~~ is independent of a layout for said second metal layer group.

30. (Currently Amended) The method as set forth in claim 28, further comprising a plurality of pre-designed circuit blocks ~~self-contained layout sections~~ in said first metal layer group.

31. (Currently Amended) The method as set forth in claim 30, wherein at least one of said pre-designed circuit blocks ~~self-contained layout sections~~ comprise a wiring direction perpendicular to a wiring direction of a second one of said pre-designed circuit blocks ~~self-contained layout sections~~.

32. (Canceled).

33. (Original) The method as set forth in claim 28, wherein said first metal layer group comprises three metal layers.

34. (Previously Presented) The method as set forth in claim 33, wherein said three metal layers comprise first, second, and third metal layers, each of said three metal layers comprising conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

35. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

36. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

37. (Currently Amended) The method as set forth in claim 28, wherein said pre-designed circuit block ~~self-contained layout section~~ comprises a layout for a memory block.

38. (Canceled).

39. (Currently Amended) The method as set forth in claim 28, wherein said pre-designed circuit block ~~self contained layout section~~ comprises a section less than 10 percent of the entire area of said metal layer in said first metal layer group.

40-50 (Cancel).